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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,108	09/09/2003	Dureseti Chidambarrao	FIS920030183US1	2107

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EXAMINER	
PHAM, LONG	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,108	CHIDAMBARRAO ET AL.	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-18 and 21-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16-18 and 21-29* is/are allowed.

6)☒ Claim(s) *1 and 3-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 3, 4, 5, 6, 12, 13, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in combination with Nayak (US 6,372,590).

With respect to claims 1, 3, 4, 5, 14, and 15, AAPA teaches a method for manufacturing a semiconductor device, comprising steps of (see the Background of Invention of this application):

forming source and drain regions in an upper surface of a SiGe-based substrate, the source and drain regions containing an n-type impurity.

AAPA fails to teach forming source and drain extension regions in the upper surface of substrate and providing a vacancy-trapping element by implanting a noble gas or nitrogen into the source and drain extension regions.

Nayak teach forming n-type source and drain extension regions in an upper surface of an substrate and then providing a vacancy-trapping element by implanting a noble gas or nitrogen with implantation dose of $1x\ 10^{14}$ to $5x\ 10^{15}$ atoms/cm^2 and implantation energy of 1KeV to 100KeV into the source and drain extension regions to reduce series resistance and hot carrier effects. See the abstract of Nayak.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to form source and drain extension regions in the upper

surface of substrate and providing a vacancy-trapping element by implanting a noble gas or nitrogen with implantation dose of 1x 10^{14} to 5x 10^{15} atoms/cm^2 and implantation energy of 1KeV to 100KeV into the source and drain extension regions to obtain above advantages.

Further with respect to claim 1, since AAPA in combination with Nayak teach providing a vacancy-trapping element by implanting a noble gas or nitrogen with implantation dose of 1x 10^{14} to 5x 10^{15} atoms/cm^2 and implantation energy of 1KeV to 100KeV into the source and drain extension regions, the vacancy concentration in the source and drain extension regions would inherently be reduced and the diffusion of the n type impurity in the source and drain extension regions would inherently be decreased.

With respect to claim 6, AAPA further teaches that the SiGe-based substrate comprises a Si cap layer on a SiGe film on a silicon substrate.

With respect to claim 12, Nayak further teaches that source and drain regions overlap the source and drain extension regions. See figs. 1j and 1k.

With respect to claim 13, Since Nayak teaches providing a vacancy-trapping element by implanting a noble gas or nitrogen with implantation dose of 1x 10^{14} to 5x 10^{15} atoms/cm^2 and implantation energy of 1KeV to 100KeV into the source and drain extension regions and since Nayak teaches that source and drain regions overlap the source and drain extension regions, a vacancy-trapping element is provided in the source and drain region.

2. Claims 7, 8, 9, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in combination with Nayak (US 6,372,590).

With respect to claims 7 and 8, Nayak fails to teach that the peak concentrations of the implanted nitrogen and n-type impurity of the source

and drain extension regions are at the same depth from the upper surface of the substrate.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range for the depth for the peak concentrations of the implanted nitrogen and impurity through routine experimentation and optimization to obtain optimal or desired device performance because the relative depths of the nitrogen and impurity are result-effective variables and there is no evidence indicating that they are critical or produce any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

With respect to claim 9, annealing is well-known to one of ordinary skill in the art of making semiconductor devices.

With respect to claim 10, the annealing temperature and duration are result-effective variables and there is no evidence indicating that they are critical or produce any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

With respect to claim 11, AAPA implicitly teaches forming a gate electrode on the upper surface of SiGe-based substrate with a gate oxide film therebetween. See the Background of Invention.

Allowable Subject Matter

3. Claims 16-18 and 21-29 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on M-F, 7:30AM-3:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Pham
Primary Examiner
Art Unit 2814

LP

1.